REMARKS

Claims 1, 2, 4, 5, 9, 10, 13-16 and 19 were pending. Claims 3, 6-8, 11, 12, 17, 18 and 20 were previously withdrawn. The Examiner rejected claims 1, 4, 9, 13, and 19 under 35 U.S.C. §102(b) as being anticipated by Lee (U.S. Patent No. 6,429,841). Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Lee and claims 2, 5 and 14-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lee in view of either Sakaguchi (U.S. Patent Publication No. 2003/0201959), Fallot-Burghardt et al. (U.S. Patent No. 7,038,646) or Medina (U.S. Patent No. 6,359,389). In response, Applicants have amended independent claims 1 and 19 to incorporate the subject matter of claim 5 and added claim 21. No new matter has been added. Therefore, claims 1, 2, 4, 9, 10, 13-16, 19 and 21 are now pending. Applicants respectfully request reconsideration of the pending claims in view of the preceding amendments and the following remarks.

Claim Rejections Under 35 U.S.C. §102 and §103

Independent Claims 1, 13, and 19

Independent claims 1 and 19 are directed to a voltage driven array having an array of discrete elements organized into at least one row and a plurality of columns. Each of claims 1 and 19 as amended include a voltage supply (or voltage supply means) "configured to supply the array with voltages in a time delay multiplexed fashion." *emphasis added.* Similarly, independent claim 13 is directed to a method for providing a variable voltage to a voltage driven array that includes "providing the first end with a first

voltage and the second end with a second voltage that is different from the first voltage to generate a voltage in each of the columns that is different from a voltage in a remainder of the columns." *emphasis added.* None of the cited references, taken alone or in combination, teach or suggest the above-recited features of claims 1, 13 and 19.

Independent Claim 13

Independent claim 13 recites a method that includes providing the first end of a resistive element with a first voltage and the second end of the resistive element with a second voltage that is different from the first voltage. The §102 reference cited by the Examiner in this case (i.e., Lee) does not teach or suggest this feature. Rather, Lee discloses a method for preventing picture distortion in a liquid crystal display apparatus that includes a horizontal electric field system liquid crystal panel in which gate lines are crossed with source lines. *Lee*, col. 7, lines 13-19; Figure 7. The liquid crystal display of Lee further includes a gate-side drive circuit connected to the gate lines, and a data-side drive circuit connected to the source lines. The gate-side circuit sequentially applies a scanning signal to the gate lines, which drives pixels on the display panel sequentially for one line. *Lee*, col. 7, lines 27-33; Figure 7. The data-side drive circuit applies a source voltage signal to each source line of the display each time the scanning signal is applied to any one of the gate lines. *Lee*, col. 7, lines 35-38. The data-side circuit also includes a plurality of source driver integrated circuits connected to the source line groups to divisionally receive voltage signal sets from a resister bus. The ends of the resistor bus are connected to a first gamma voltage generator and a second gamma voltage

generator, respectively. The first gamma voltage generator generates a first voltage signal set to be applied to one end of the resistor bus, while the second voltage generator provides a second voltage signal set to another end of the resistor bus. "The first gamma voltage signal set has a voltage level equal to that of the second gamma voltage signal set." *Lee*, col. 7, lines 45-64. *emphasis added.* In other words, the first and second voltages at each end of the resistor bus are the same. Therefore, Lee cannot possibly teach or suggest a voltage driven array that includes "providing the first end with a first voltage and the second end with a second voltage that is different from the first voltage," as recited in independent claim 13. For at least this reason, claim 13 is patentable over Lee and in condition for allowance.

Independent Claims 1 and 19

Independent claims 1 and 19 were amended to incorporate the subject matter of dependent claim 5, which was rejected under §103 as being unpatentable over Lee in view of Fallot-Burghardt. As the Examiner concedes (Office Action, pages 4-5, item 6), "Lee fails to disclose that the array is supplied with voltages in a time delay multiplexed fashion" and looks to Fallot-Burghardt to cure this deficiency. Applicants respectfully submit, however, that Fallot-Burghardt also fails to teach or suggest this recited feature of claims 1 and 19.

Fallot-Burghardt discloses a circuit arrangement for calibration of a liquid crystal display device. *Fallot-Burghardt*, col.1, lines 7-10. The circuit arrangement includes a voltage divider having a plurality of series-connected resistors and having voltage pick-offs arranged between the resistors for picking off different voltage levels. A single one

of the voltage pick-offs is provided with means for fine-tuning the voltage level pick-off. *Fallot-Burghardt*, col.2, lines 54-62. In other words, a single one of the voltage pick-offs is designed so that the voltage level picked off at that particular contact is capable of fine-tuning. *Fallot-Burghardt*, col.4, lines 24-27. Each pick-off contact is connected to a respective input of a static analog multiplexer that is controlled by a read-only memory programmable once or repeatedly. In this way, once found, the optimum fine-tuning voltage level is stored. *Fallot-Burghardt*, col.5, lines 15-28. This calibration is performed once for each individual circuit by the circuit manufacturer or by the manufacturer of the liquid crystal display device. *Fallot-Burghardt*, col.5, lines 11-13. Therefore, the calibration method of Fallot-Burghardt is wholly unrelated to time delay multiplexing and cannot possibly teach or suggest an array that is supplied with voltages in a time delay multiplexed fashion, as recited in amended claims 1 and 19. Accordingly, for at least this reason, independent claims 1 and 19 are patentable over the cited art and in condition for allowance.

CONCLUSION

Reconsideration and allowance are respectfully requested. In view of the above, each of the presently pending claims in this application is believed to be in condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicant believes any fee due has been addressed in the accompanying transmittal charging Deposit Account No. 08-2025, under Order No. 200311998-1 from which the

undersigned is authorized to draw. To the extent necessary, a petition for extension of time under 37 C.F.R. § 1.136 is hereby made, the fee for which should be charged to such deposit account number.

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Respectfully submitted,

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